



SHEET 1 OF 1

<b>INFORMATION DISCLOSURE CITATION</b>  PTO-1449		ATTY. DOCKET NO. SUN-P9324-MEG		APPLICATION NO. 10/637,165			
		APPLICANT Marc Tremblay, et al.					
		FILING DATE 08 August 2003		GROUP ART UNIT 2122 2109			
		<b>U.S. PATENT DOCUMENTS</b>					
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
<b>FOREIGN PATENT DOCUMENTS</b>						Translation	
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Yes	No
/MZ/	WO 01 93028 A2	6 December 2001	PCT				
/MZ/	WO 03/054693	3 July 2003	PCT				
<b>OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)</b>							
/MZ/	"The Potential for Using Thread-Level Data Speculation to Facilitate Automatic Parallelization", by J. Gregory Steffan et al., 1998, IEEE, Pages 2-13.						
EXAMINER	/Meng Yao Zhe/		DATE CONSIDERED		04/11/2007		

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<b>OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)</b>						
/MZ/	"Lock-Based Programs and Transactional Lock-Free Execution", by Ravi Rajwar et al., University of Wisconsin-Madison Technical Report #1440, April 2002.					
/MZ/	"Speculative Locks for Concurrent Execution of Critical Sections in Shared-Memory Multiprocessors", by Jose F Martinez et al., Workshop on Memory Performance Issues, International Symposium on Computer Architecture, June 2001.					
/MZ/	"Transactional Memory: Architectural Support for Lock-Free Data Structures", by Maurice Herlihy.					
/MZ/	"Speculative Locks for Concurrent Execution of Critical Sections in Shared-Memory Multiprocessors", by Jose F. Martinez et al., Technical Report UIUCDCS-R-2001-2202, February 2001.					
/MZ/	"Transactional Lock-Free Execution of Lock-Based Programs", by Ravi Rajwar, Proceedings of the Tenth International Conference on Architectural Support for Programming Languages and Operating Systems, Oct. 6-Oct. 9, 2002, San Jose, CA.					
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						Yes
<b>OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)</b>						
/MZ/	Publication: "Speculative Synchronization: Applying Thread-Level Speculation to Explicitly Parallel Applications" by Jose F. Martinez and Josep Torrellas, Dept. of Computer Science, University of Illinois at Urbana-Champaign, Urbana, IL 61801 USA, <a href="http://iacoma.cs.uiuc.edu">http://iacoma.cs.uiuc.edu</a> , XP-002285169, published in ASPLOS X, 10-2002, Pgs. 18-29.					
/MZ/	Publication: "Speculative Lock Elision: Enabling Highly Concurrent Multithreaded Execution" by Ravi Rajwar and James R. Goodman, Computer Sciences Department, University of Wisconsin-Madison, Madison, WI 53706 USA, <a href="mailto:rajwar@cs.wisc.edu">rajwar@cs.wisc.edu</a> , XP-001075852, published in IEEE Journal 1-12-2001, Pgs. 294-305.					
/MZ/	Publication: "Transactional Memory: Architectural Support for Lock-Free Data Structures" by Maurice Herlihy, Digital Equip. Corp. Cambridge Research Laboratory, Cambridge, MA 02139, <a href="mailto:herlihy@crl.dec.com">herlihy@crl.dec.com</a> and J. Eliot B. Moss, Dept. of Computer Science, University of Massachusetts, Amherst, MA 01003, <a href="mailto:moss@cs.umass.edu">moss@cs.umass.edu</a> , XP-000380375, published in Computer Architecture News, May 21, 1993, Pgs. 289-300.					
/MZ/	Publication: "Enhancing Software Reliability with Speculative Threads" by Jeffrey Oplinger and Monica S. Lam, Computer Systems Laboratory, Stanford University, <a href="mailto:jeffop@stanford.edu">jeffop@stanford.edu</a> , XP-002285168 published in ASPLOS X, 10-2002, Pgs. 184-196					
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## INFORMATION DISCLOSURE CITATION

PTO-1449

ATTY. DOCKET NO.  
SUN-P9324

APPLICATION NO.  
10/637,165

APPLICANT  
Marc Tremblay, et al.

FILING DATE  
08 August 2003

GROUP ART UNIT  
~~2122~~ 2109

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EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
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						Yes No

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/MZ/	Publication entitled "Speculation-Based Techniques for Transactional Lock-Free Execution of Lock-Based Programs", by Ravi Rajwar, Online! 2002, XP002286237, Retrieved from the internet: URL: <a href="http://bbc.uwaterloo.ca/{brecht/courses/856/readings-new/rajwar02speculationsbased.pdf">http://bbc.uwaterloo.ca/{brecht/courses/856/readings-new/rajwar02speculationsbased.pdf}</a>
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EXAMINER	/Meng Yao Zhe/	DATE CONSIDERED	04/11/2007
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## SHEET 2 OF 3

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<b>U.S. PATENT DOCUMENTS</b>					
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS
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/MZ/	6,681,311	01-2004	Gaskins, et al.	711	203
<b>FOREIGN PATENT DOCUMENTS</b>					
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS
<b>OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)</b>					
/MZ/	Publication entitled "Improving the Throughput of Synchronization by Insertion of Delays", by Ravi Rajwar et al. Proceedings of the Sixth International Symposium on High-Performance Computer Architecture, 8-12 January 2000, Pages 168-179.				
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/MZ/	Publication entitled "Multi-view Memory to Support OS Locking For Transaction Systems", P. Bodorik et al., IEEE, 1997, Pages 309-318.				
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<b>FOREIGN PATENT DOCUMENTS</b>						
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						Yes No
<b>OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)</b>						
/MZ/	"Structured Computer Organization" by Andrew S. Tanenbaum, Published 1999, pages 5, 7-8					
/MZ/	"The Transaction Concept: Virtues and Limitations" by Jim Gray. Pro. Int'l Conf. Very Large Databases, Morgan Kaufman, 1981. pages 144-154					
/MZ/	"Toward Efficient and Robust Software Speculative Parallelization on Multiprocessors" by Marcelo Cintra and Diego R. Lianos, PPoPP' 03 June 11-13, 2003 ACM 1-58113-588-2/03/0006 pages 13-24.					
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